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Selected US specifications from IPC sub-class H04N

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(54) Solid state image pick-up arrangement

(57) A solid state image pick-up device comprises an image sensing part 1 having a plurality of sensing cells arranged in at least one line for producing electrical information in response to incident radiation; a read-out part 31–33 for reading out said electrical information produced by said image sensing part, said read-out part including m separate read-out channels, where m is an integer no smaller than three; and a storage part 2 disposed between said image sensing part and said read-out part for classifying the electrical information in one line of said image sensing part into m groups and supplying the respective groups of electrical information to said read-out part in time-sharing. The storage part includes storage cells classified into groups each comprising m adjacent cells. One direct channel and (m−1) delay channels 17 are connected to each storage cell group, the (m−1) delay channels being arranged to connect (m−1) storage cells to the direct channel to which the remaining cell of the respective group is connected. The direct channel in each group is connected to the read-out part. A colour stripe filter is disposed in front of the image sensing part having a pitch coincident with the pitch of the sensing cells thereof.

FIG. 7

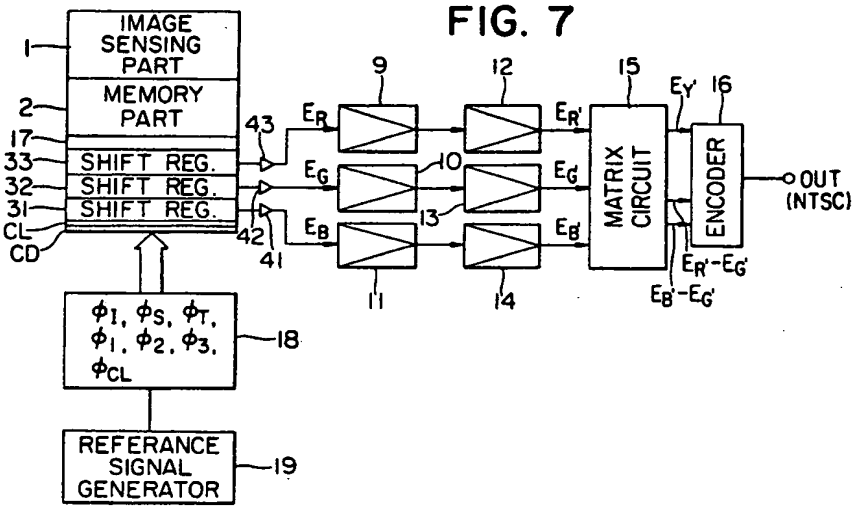

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FIG. 1 PRIOR ART

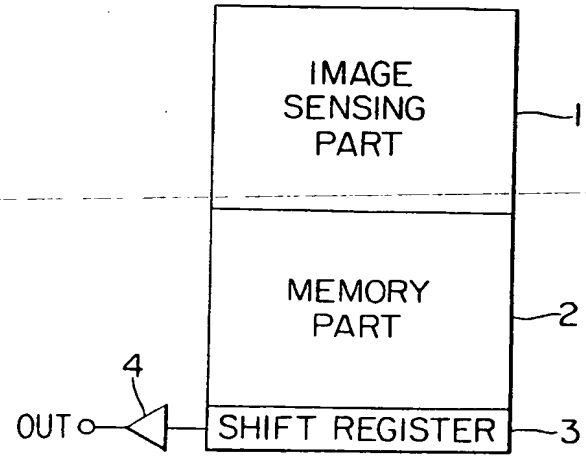


FIG. 2
PRIOR ART

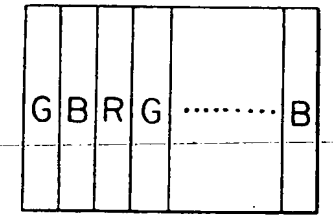


FIG. 4

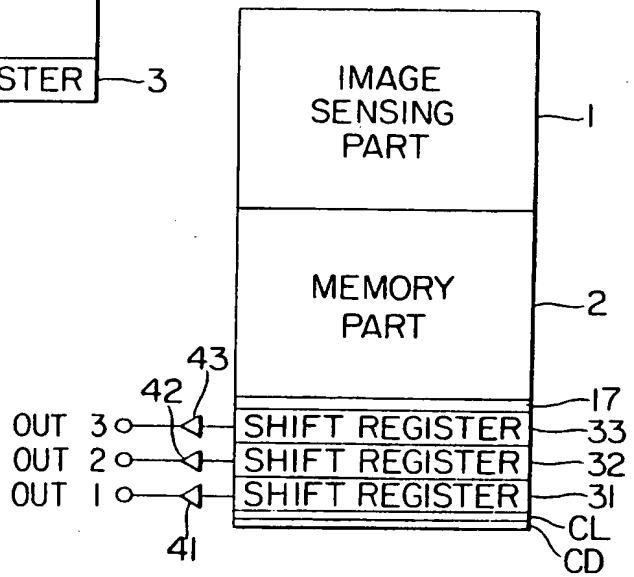


FIG. 3 PRIOR ART

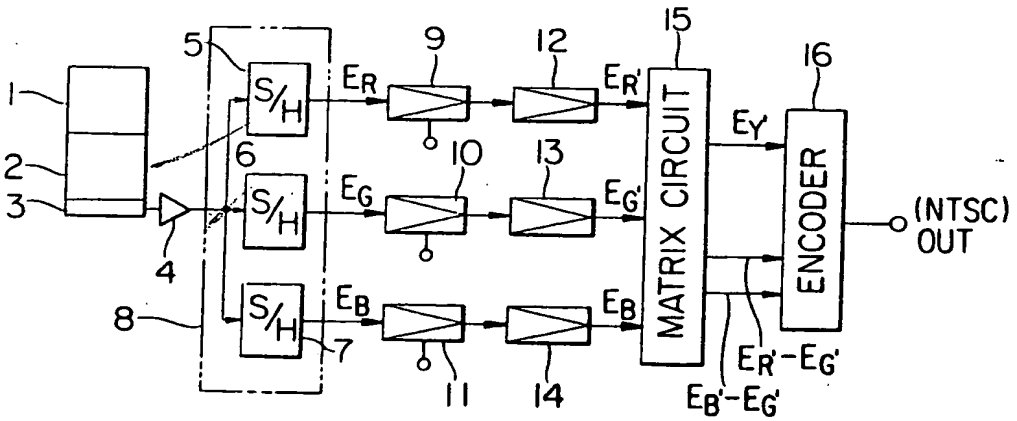
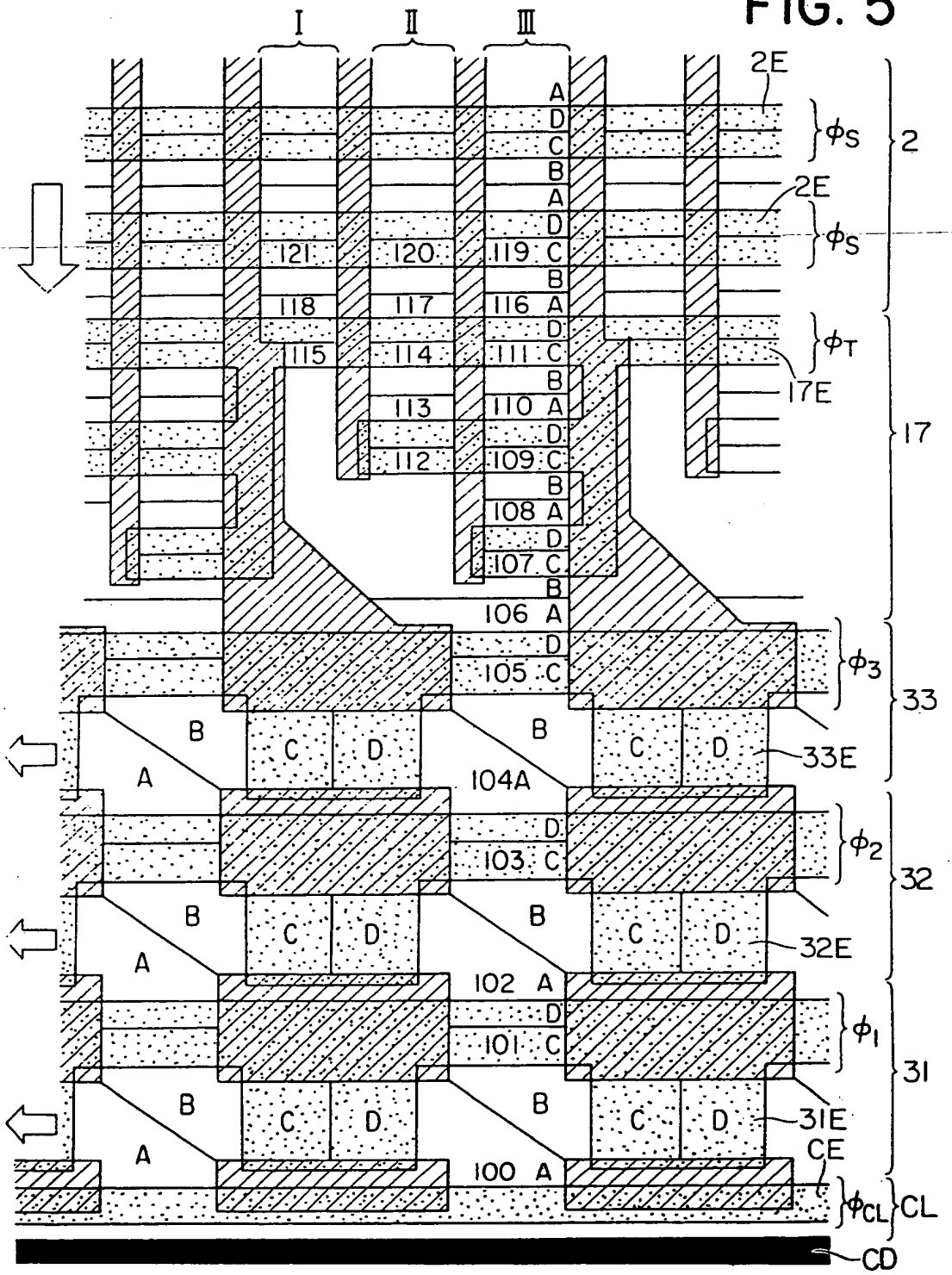


FIG. 5


I
II
III
2E
A
D
C
B
A
ϕ_S
2
2E
ϕ_S
121
120
119 C
118
117
116 A
ϕ_T
115
114
111 C
17E
113
110 A
17
112
109 C
108 A
107 C
106 A
D
105 C
ϕ_3
33
B
C
D
A
104A
33E
ϕ_2
103 C
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32E
102 A
ϕ_1
101 C
31
31E
CE
100 A
ϕ_{CL}
CL
CD

FIG. 6A

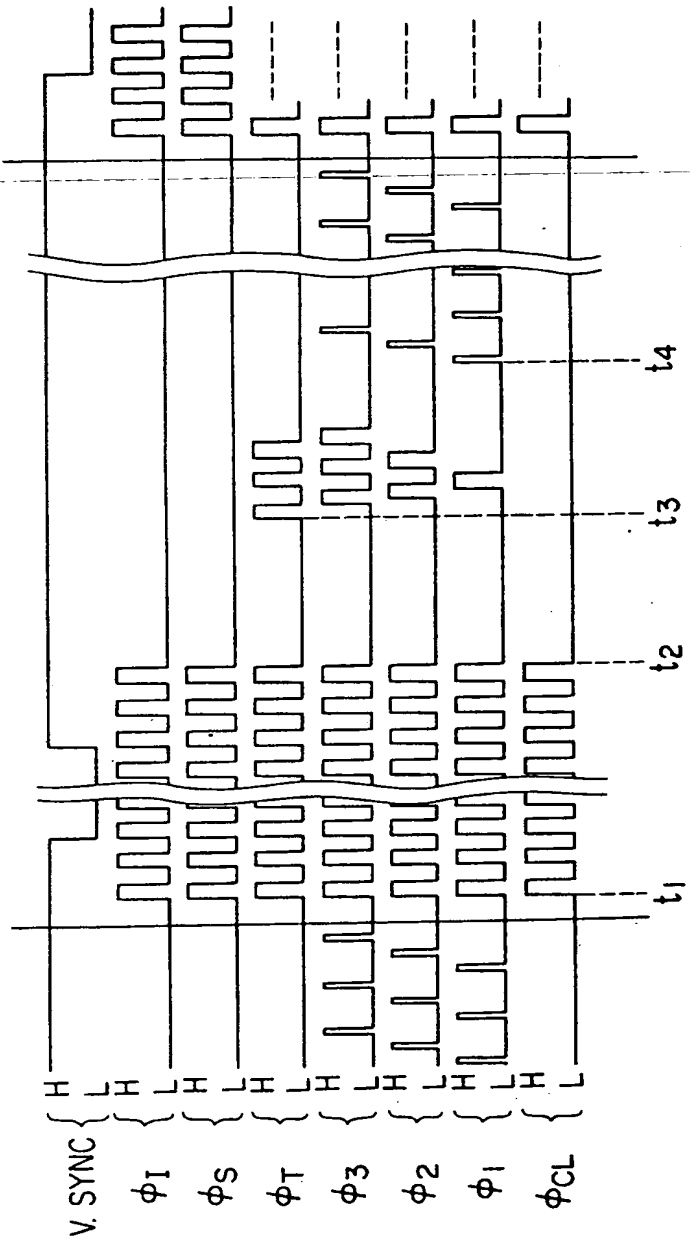


FIG. 6B

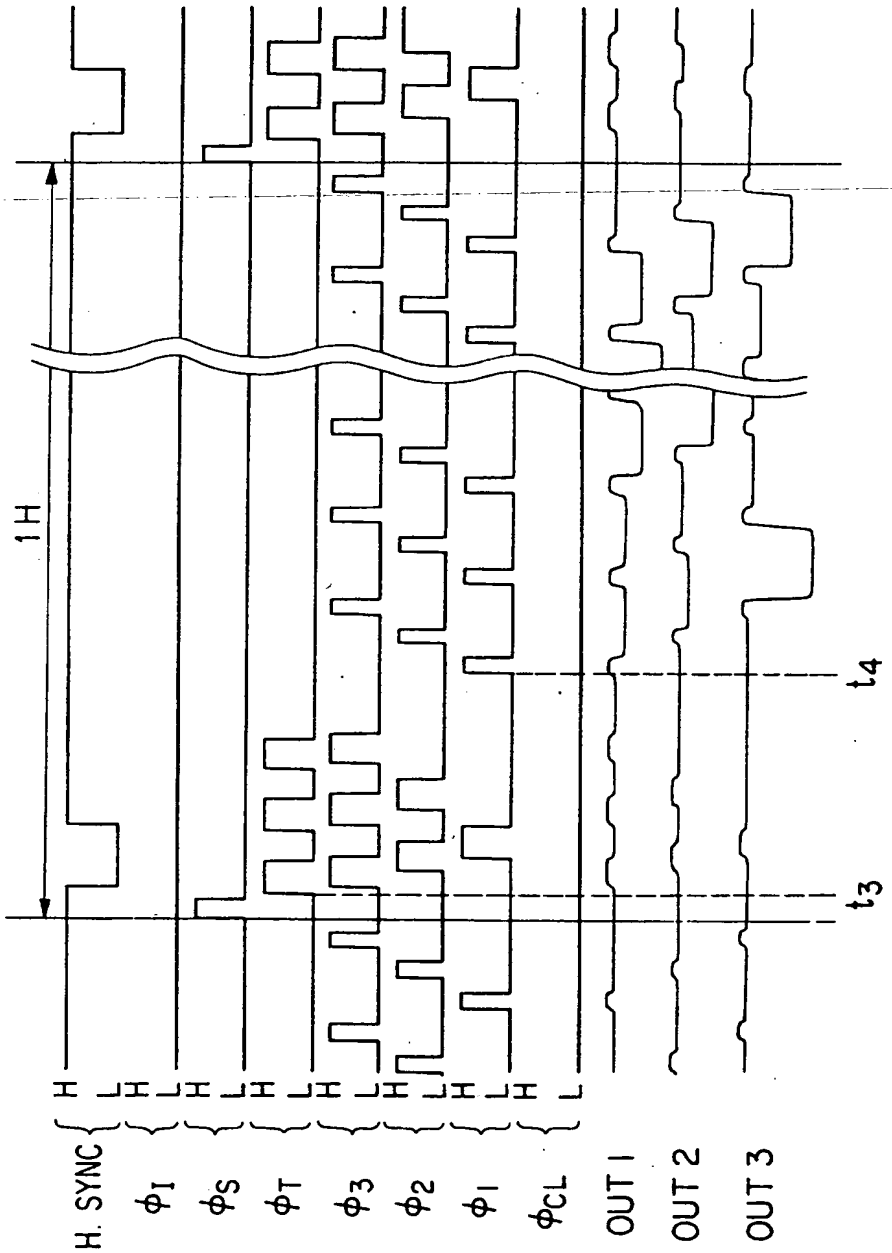
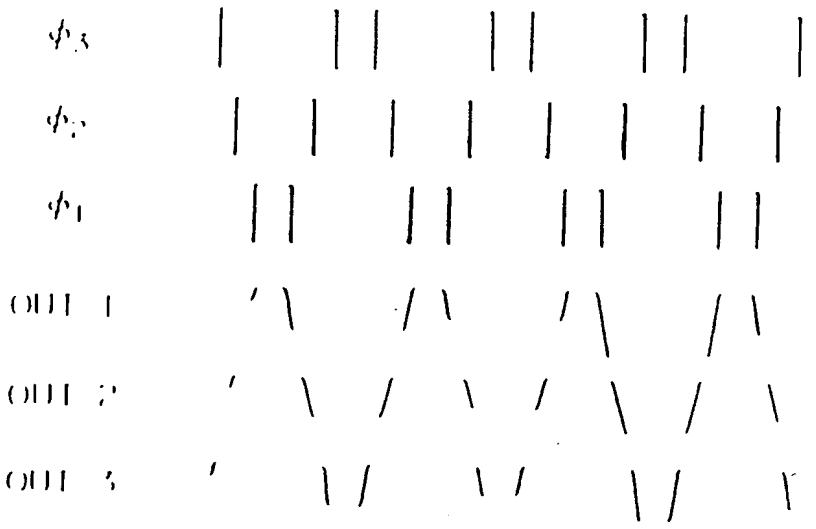

1H
t4
t3
H
L
H. SYNC
ϕ_I
ϕ_S
ϕ_T
ϕ_3
ϕ_2
ϕ_1
ϕ_{CL}
OUT 1
OUT 2
OUT 3

FIG. 6C



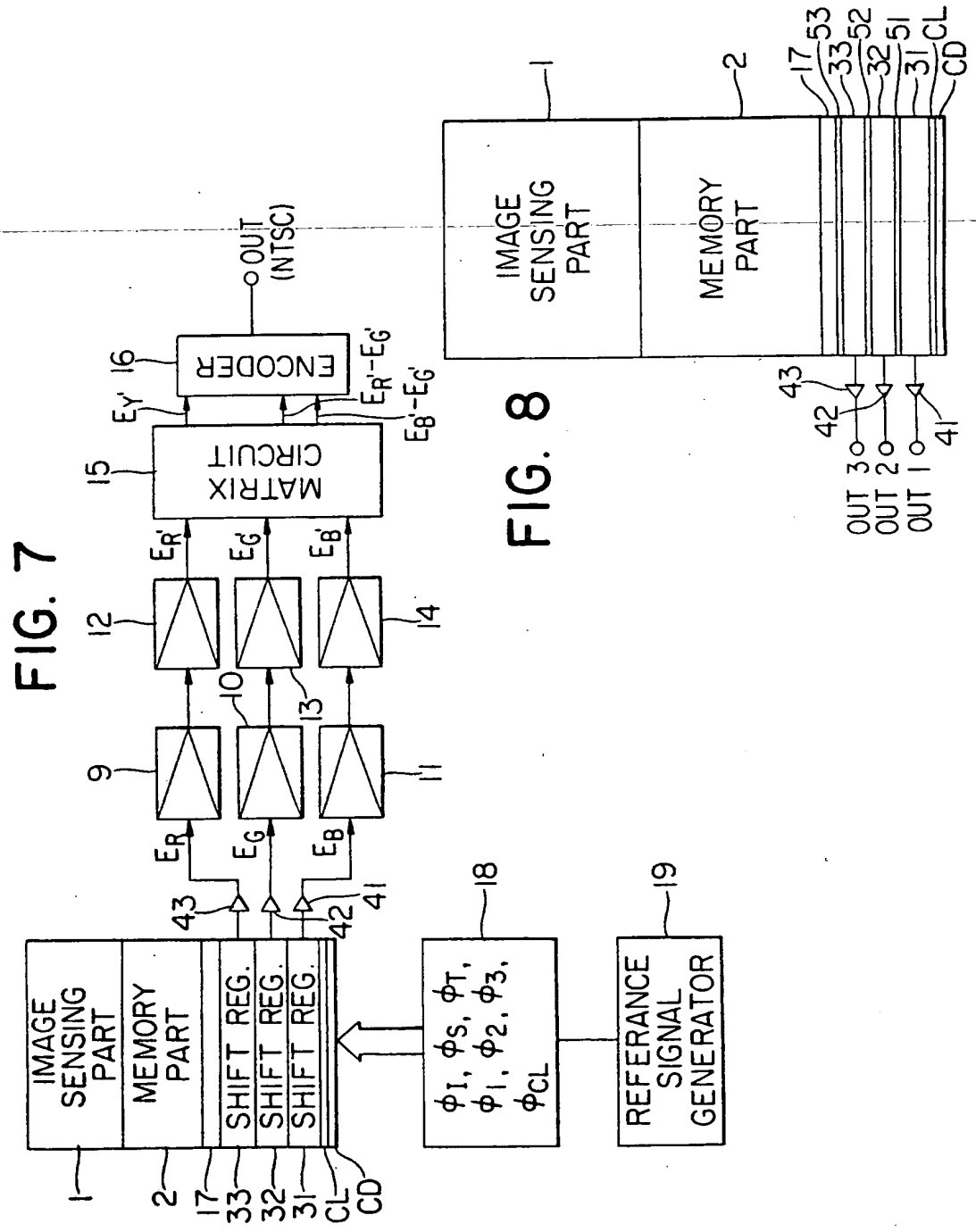


IMAGE SENSING PART
MEMORY PART
SHIFT REG.
SHIFT REG.
SHIFT REG.
REFERANCE SIGNAL GENERATOR
MATRIX CIRCUIT
ENCODER
OUT (NTSC)
1
2
17
33
32
31
CL
CD
53
52
51
41
42
43
9
10
11
12
13
14
15
16
18
19
OUT 1
OUT 2
OUT 3

FIG. 7

FIG. 8

FIG. 9

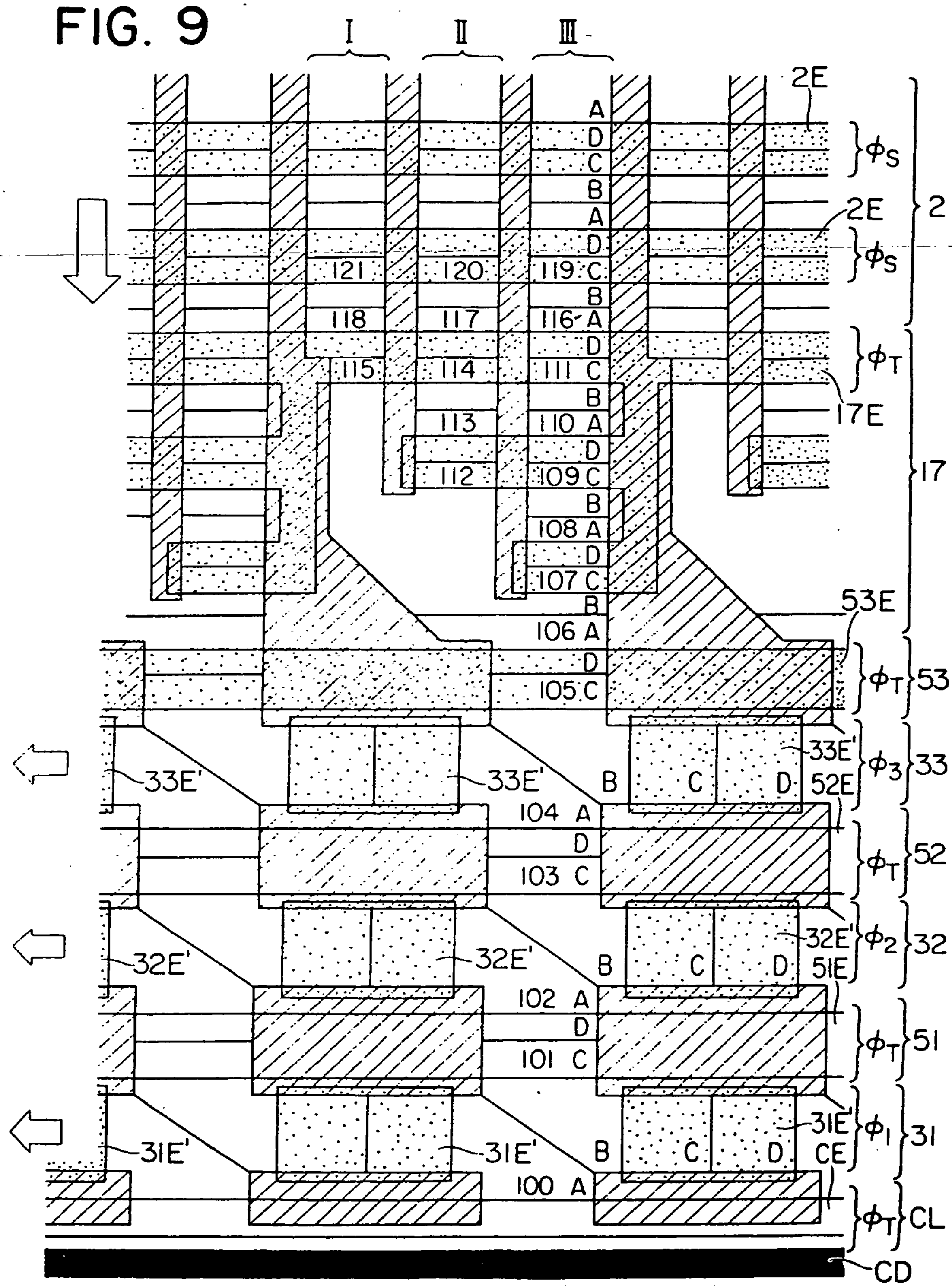

I
II
III
2E
φS
2
φT
17E
17
53E
φT
53
33E'
φ3
33
52E
φT
52
32E'
φ2
32
51E
φT
51
31E'
φ1
31
CE
φT
CL
CD
121
120
119
118
117
116
115
114
111
113
110
112
109
108
107
106
105
104
103
102
101
100
A
B
C
D

FIG. 10A

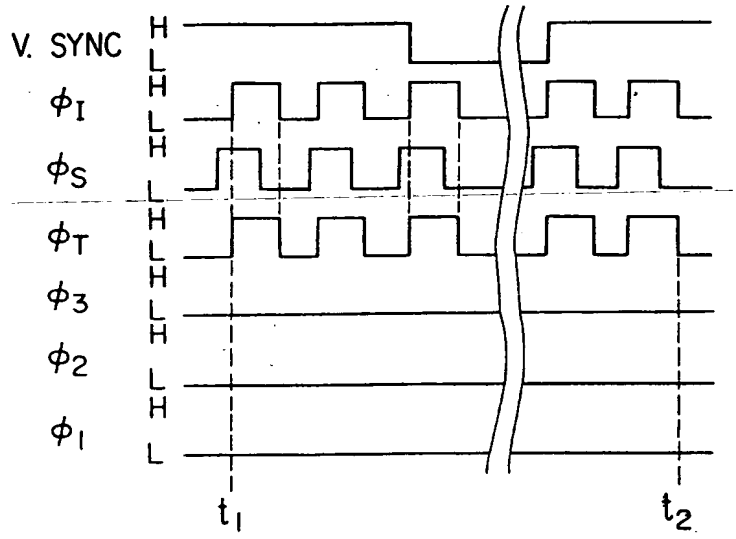


FIG. 10B

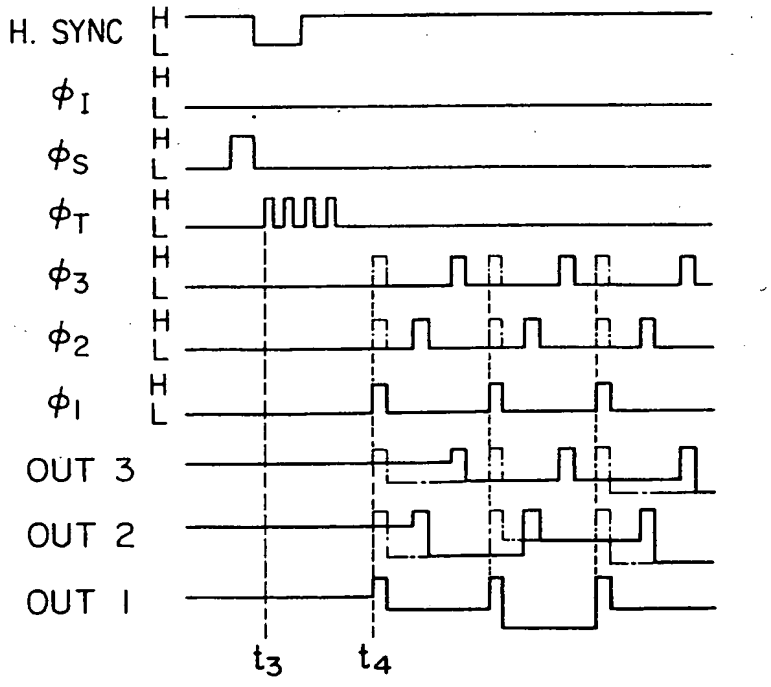
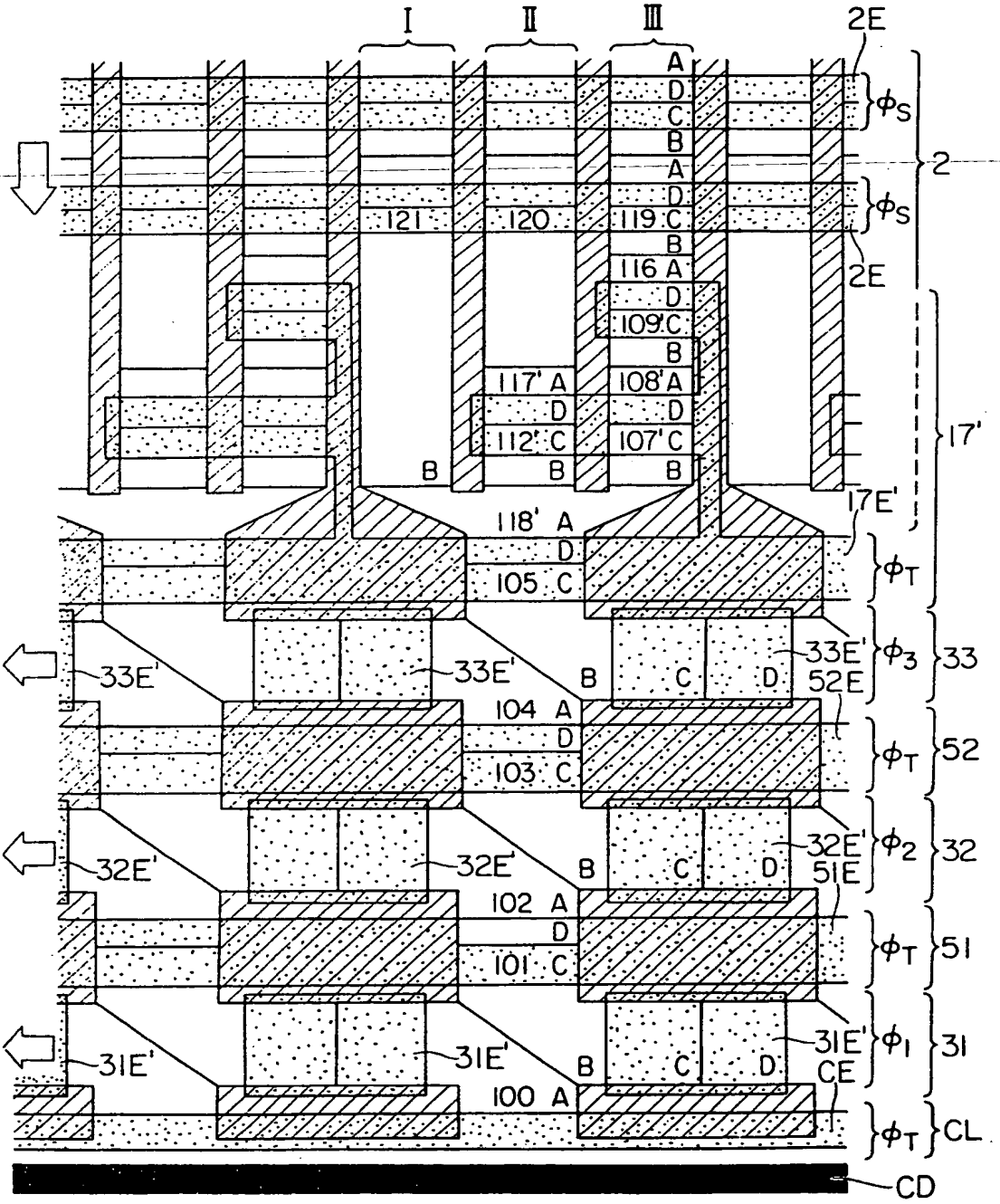


FIG. 11


I
II
III
2E
A
D
C
B
A
D
C
B
ϕ_S
2
121
120
119
116
109'
117'
108'
112'
107'
17'
17E'
118'
105
ϕ_T
33E'
ϕ_3
33
52E
104
103
52
32E'
ϕ_2
32
51E
102
101
51
31E'
ϕ_1
31
CE
100
CL
CD

SPECIFICATION

Solid state image pick-up device and image pick-up system using the same

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a solid state image pick-up device and an image pick-up system using the same, and more particularly to a solid state image pick-up device and an image pick-up system suitable to produce a color image signal.

Description of the Prior Art

In the prior art, when a color image signal with three or more color signals are to be produced by one or two solid state image pick-up devices, image sensing parts of the image pick-up devices receive lights through color separating optical members such as color filters arranged in stripe or mosaic to form electrical information representative of the respective colors in picture cells and the electrical information of the picture cells are time-serially read out through a common transfer path.

Fig. 1 shows an example of a well-known prior art solid state image pick-up device which utilizes a frame transfer (FT) type charge coupled device (CCD).

In Fig. 1, numeral 1 denotes an image sensing part having a plurality of photo-electric converting picture cells arranged in rows and columns. Numeral 2 denotes a memory part having a plurality of memory cells arranged in rows and columns for storing charge information of the picture cells of the image sensing part 1. Numeral 3 denotes a horizontal register which functions as a read-out transfer path for reading out the information of the memory part 2 one horizontal line at a time and for transferring the line information horizontally to time-serially produce dot-sequential signals.

By arranging a color separating filter of stripe type as shown in Fig. 2 in front of the image sensing part 1 with a pitch of the color filter portions R (red), G (green) and B (blue) being coincident with a pitch of the picture cells of the image sensing part 1, the picture cells in the respective columns produce signals representative of the respective colors and the point-sequential color signals are time-serially produced from the horizontal shift register 3.

The color signals thus produced are converted into, for example, a color video signal according to an NTSC system by a signal processing circuit as shown in Fig. 3.

The dot-sequential image output signals from a CCD amplifier 4 are sampled and held by a signal separation circuit 8 comprising three sample and hold circuits 5, 6 and 7 so that a red signals E_R, a green signal E_G and a blu signal E_B are separated. The color signals E_R, E_G and E_B are level-adjusted by variabl gain amplifiers 9, 10 and 11, respectively, so that a white balance is controlled. The level-adjusted color signals are then processed by processing circuits 12, 13 and 14 each including, for example, a clamp circuit, a gamma correction circuit and an aperture correction circuit, etc., and the signals are converted into a luminance signal and a color difference signal by a matrix circuit 15, and they are converted into the color video signal by an encoder 16.

With such an arrangement, the horizontal register 3 sequentially reads out three primary colors. In order to read out them with a carrier of 3.58 MHz, a clock of 3.58 MHz × 3 = 10.74 MH z is required. However, as the clock frequency is high, a signal transfer efficiency at the register 3 is reduced and a power consumption increases. As a result, a problem is encountered when the number of picture cells of the horizontal shift register or the number of horizontal picture cells of the image sensing part 1 is increased. According to an aspect of the present invention, there is provided a charge transfer image pick-up device for image signal processing, comprising:

an image sensing portion having a plurality of sensing cells arranged in at least one line for producing electrical information in response to incident radiation;

a storage portion having at least one row of n storage cells each for storing an electrical charge in response to a respective one of the sensing cells, said one row being classified into a plurality of storage cell groups each comprising m adjacent cells, m being no smaller than three;

one direct channel and (m-1) delay channels for each storage cell group, the (m-1) delay channel being arranged to connect (m-1) storage cells to the direct channel to which the remaining cell of the respective group is connected, each channel providing a different amount of delay; and

a read-out portion for reading out the electrical charges of one row of said storage portion and arranged to receive those electrical charges through said direct channel in each group.

For a better understanding of the present invention, reference will now be made by way of example, to the accompanying drawings in which:

Figure 1 shows a configuration of a prior art frame transfer type CCD,

Figure 2 shows an example of a stripe color filter,

Figure 3 shows a configuration of a prior art color image signal processing circuit,

Figure 4 shows one embodiment of a solid state image pick-up device of the present invention,

Figure 5 shows detail of the device of Fig. 4,

Figures 6A, 6B and 6C show an exampl of

a vertical transfer timing and two examples of a horizontal transfer timing of the device, respectively,

Figure 7 shows a configuration of a color image pick-up system which uses the image pick-up device shown in Figs. 4 and 5,

Figure 8 shows another embodiment of the solid state image pick-up device of the present invention,

Figure 9 shows detail of the device of Fig. 8,

Figures 10A and 10B show a vertical transfer timing and a horizontal transfer timing of the device of Fig. 8, and

Figure 11 shows a further embodiment of the solid state image pick-up device of the present invention, shown in a similar manner to Figs. 5 and 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One embodiment of the present invention is shown in Fig. 4 in which the like numerals to those shown in Figs. 1 and 3 denote the like elements or like functional means.

In Fig. 4, a color stripe filter for color separation as shown in Fig. 2 is arranged in front of the image sensing part 1. Numerals 31, 32 and 33 denote horizontal shift registers which function as horizontal readout sections, numerals 41, 42 and 43 denote charge voltage conversion amplifiers, and numeral 17 denotes separating input section arranged between the memorgy part 2 and the three horizontal shift registers 31–33 for distributing three color information contained in the last one horizontal line of the memory part 2 to the corresponding one of the three horizontal shift registers 31–33 through parallel-to-serial conversion of the charges.

In the present embodiment, three horizontal shift registers 31–33 are provided, one for each of the color signals to be produced, as the readout transfer paths and the charges representative of the respective colors are distributed to the respective horizontal shift registers 31, 32 and 33 to read out the information.

Accordingly, the respective color signals are essentially sampled by the horizontal registers 31, 32 and 33 and the amplifiers 41, 42 and 43 produce the separated color signals simultaneously.

A charge clear drain CD is arranged at the lowermost end of the image pick-up device, that is, under a charge clear gate CL adjacent to the horizontal shift register 31. The drain CD is connected to a power source circuit.

Fig. 5 shows an electrode structure f the image pick-up devic f Fig. 4. It shows a lower end of th memory part 2 and the three horizontal shift registers 31–33.

Hatched areas sh w channel st ps, numerals 31E–33E d not s transfer electrod s of the horizontal shift registers 31–33, num ral 17E denotes a transfer electrode of the separating unit section 17 and numeral 2E denotes a transfer electrode of the memory part 2.

While the present embodiment shows a single-phase driven transfer, two-phase, three-phase or even four-phase driven transfer may be used.

A set of portions A, B, C and D form a unit cell and potentials of the portions A-D are represented by P(A)-P(D). Virtual electrodes are formed by ion injection such that P(A)<P(B) and potential levels are fixed. Potentials of the portions C and D under the transfer electrodes are set such that P(C)<P(D). When low level voltages are applied to the respective electrodes, a relation of P(A)<P(B)<P(C)<P(D) is met, and when high level voltages are applied, a relation of P(C)<P(D)<P(A)<P(B) is met.

$\phi 1$-$\phi 3$ denote clock pulses applied to the electrodes 31E–33E, ϕT denotes a clock pulse applied to the electrode 17E, ϕS denotes a clock pulse applied to the electrode 2E and ϕCL denotes a clock pulse applied to the electrode CE of the clear gate CL.

Figs. 6A and 6B show a vertical transfer clock timing and a horizontal transfer timing, respectively.

Fig. 7 shows a block diagram of a color image pick-up system which uses the image pick-up device shown in Figs. 4 and 5. Numeral 18 denotes a driver which functions as control means and supplies the clock pulses ϕI, ϕS, ϕT, $\phi 1$, $\phi 2$, $\phi 3$ and ϕCL as shown in Figs. 6A and 6B. ϕI denotes the clock pulse applied to the electrode of the image sensing part 1. Numeral 19 denotes a reference signal generator. The like numerals to those shown in Fig. 3 denote the like elements. A seen from Fig. 7, the present embodiment omits the sample and hold circuit for separating the color information so that the circuit configuration is simplified.

The operation of the configuration shown in Fig. 5 is explained. In the vertical transfer of the charges from the image sensing part 1 to the memory part 2 as shown in Fig. 6A, synchronized clock pulses of substantially same phase (except the clock pulse ϕS which slightly leads to the other clock pulses as shown), which are equal in number to at least the number of vertical picture cells of the image sensing area 1 are supplied in synchronism with a vertical synchronizing signal V.SYNC during a time period t_1-t_2 as the clock pulses ϕI, ϕS, ϕT, $\phi 3$, $\phi 2$, $\phi 1$ and ϕCL so that the charges remaining in the memory part 2 are drained to the clear drain CD through the horizontal registers 33, 32 and 31 and th clear gate CL and the charges in the image sensing part 1 are transferred to the mem ry part 2 and stored therein. At and after time t_3, the clock puls s ϕT, $\phi 3$, $\phi 2$ and $\phi 1$ ar supplied as shown s that the horizontal inf r-mation in the last line of the mem ry part 2

are distributed to the three horiz ntal shift registers 31–33 through the separating input section 17, and at and after time t_4, the information in the horizontal registers 31, 32 and 33 are sequentially read out by supplying the clock pulses $\phi 1$, $\phi 2$ and $\phi 3$ to the horizontal registers 31–33 as shown.

Regarding the information in the next and following lines of the memory part 2, the clock pulse ϕS is applied immediately before the time t_3 to shift one line of information to be read to the last line of the memory part 2 and then the above operation is repeated (Fig. 6B).

The operation during the time period t_3-t_4, that is, the operation to distribute the information in the last one line of the memory part 2 to the three horizontal shift registers 31–33 through the separating input section 17 is now explained in detail with reference to Figs. 5, 6A and 6B. For the sake of simplification, the shift of the charge information in only three columns I, II and III of the memory part 2 shown in Fig. 5 is explained although the same operations are carried out for the columns of other three-column sets.

At time t_3, the clock pulse ϕT assumes a high level in substantial synchronism with the horizontal synchronizing signal H.SYNC and the charges stored in the portions 116, 117 and 118 in the last one line of the memory part 2 are shifted to portions 111, 114 and 115 in the separating input section 17. When the clock pulse ϕT thereafter assumes a low level, the charges in the portions 111, 114 and 115 are shifted to portions 110, 113 and 106, respectively. When the clock pulse ϕ_3, ϕ_2 and ϕ_1 are sequentially applied slightly later than the clock pulse ϕT, the charge in the portion 106 of the separating input section 17, that is, the charge initially stored in the portion 118 in the column I of the memory part 2 is shifted to a portion 100 of the horizontal register 31 through portions 105 and 104 of the horizontal register 33, portions 103 and 102 of the horizontal register 32 and a portion 101 of the horizontal register 31 and stored in the portion 100 of the horizontal register 31.

When the clock pulse ϕT is again applied, the charges in the portions 110 and 113 of the separating input section 17 are shifted to the portions 108 and 106 through the portions 109 and 112. When the clock pulses ϕ_3 and ϕ_2 are sequentially applied slightly later than the clock pulse ϕT, the charge in the portion 106 of the separating input section 17, that is, the charge initially stored in the portion 117 in the column II of the memory part 2 is shifted to the portion 102 of the horizontal register 32 through the portions 105, 104 and 103 and stored in the portion 102.

When the clock pulse ϕT is again applied, the charg in the portion 108 of the separating input section 17 is shift d to the portion 106 through the portion 107. When the clock pulse ϕ_3 is applied slightly later than the clock pulse ϕT, the charge in the portion 106 of the separating input section 107, that is, the charge initially stored in the portion 116 in the column III of the memory part 2 is shifted to the portion 104 of the horizontal register 33 through the portion 105 and stored therein.

In this manner, the charges stored in the last one line of the memory part 2 are distributed to the groups of the columns I, II and III through the separating input part 17. Thus, if the R, G and B filter portions of a color stripe filter are arranged such that the R filter portions correspond to the column I group, the G filter portions correspond to the column II group and the B filter portions correspond to the column III group, the charges corresponding to R, G and B are stored in the horizontal registers 31, 32 and 33, respectively.

At and after the time t_4, the charges stored in the horiziontal registers 31, 32 and 33 are read out (OUT1-OUT3 in Fig. 6B).

When the charges in one horiziontal line of the memory part 2 have been read out through the horizontal registers 31–33, the clock pulse ϕS is applied to the memory part 2 as shown in Fig. 6B and the charges stored in the respective horizontal lines are vertically shifted by one horizontal line so that new charges are stored in the last one line, and then the operation of the time period t_3-t_4 is carried out to distribute the new one line of charges to the horizontal registers 31–33.

By repeating the above operations, the charges stored in the respective lines of the memory part 2 are separated to the respective colors and read out.

In order to prevent the charges of the registers 31, 32 and 33 from being mixed when the charges of the horizontal registers 31–33 are horizontally shifted, control gates for isolating the registers 31, 32 and 33 from each other in the horizontal charge transfer mode may be additionally provided as shown in another embodiment to be described later, or the waveforms of the clock pulses ϕ_1, ϕ_2 and ϕ_3 in the horizontal transfer mode may be slightly modified so that the charges are horizontally transferred without being mixed among the horizontal registers 31–33 without adding the isolating means. For example, at the time t_4, the clock pulse ϕ_3 is set to the high level in advance to the clock pulse ϕ_2 and ϕ_1 to shift the charge stored in the portion 104 of the horizontal register 33 to the portion corresponding to C under the left adjacent electrode 33E, and the clock pulse ϕ_2 is then set to the high level while keeping the clock pulse ϕ_3 at the high lev l to shift the charge stored in the portion 102 of the horizontal register 32 to the portion corresponding to C under the left adjacent electrod 32E, and the clock pulse ϕ_1 is then set to the high level

while keeping the clock pulses ϕ_3 and ϕ_2 at the high level to shift the charge stored in the portion 100 of the horizontal register 31 to the portion corresponding to C under the left adjacent electrode 31E, and the clock pulse ϕ_1 is then set to the low level in advance to the clock pulses ϕ_2 and ϕ_3 to shift the charge stored in the portion corresponding to C under the electrode 31E of the horizontal register 31 to the portion corresponding to A on the left side thereof, and the clock pulse ϕ_2 is then set to the low level to shift the charge stored in the portion corresponding to C under the electrode 32E of the horizontal register 32 to the left adjacent portion, and the clock pulse ϕ_3 is then set to the low level to shift the charge stored in the portion corresponding to C under the electrode 33E of the horizontal register 33 to the portion corresponding A on the left side thereof. In this manner, the transfer of the charges from the portions A to the portions C is carried out sequentially from the horizontal register 33 through the horizontal register 32 to the horizontal register 31, and the transfer of the charges from the portions C to the portions A is carried out in the opposite sequence from the horizontal register 31 through the horizontal register 32 to the horizontal register 33. Thus, the charges are horizontally transferred without being mixed among the horizontal registers 31–33 without the additional isolating means. The clock pulses ϕ_1, ϕ_2 and ϕ_3 and the three outputs derived are shown in Fig. 6C.

Another embodiment of the present invention is now explained. As described above, in the present embodiment, controllable isolate sections for isolating the horizontal registers 31, 32 and 33 from each other in the horizontal charge transfer mode is additionally provided.

Referring to Fig. 8, the like numeral to those shown in the previous drawings designate the like elements. Numerals 51, 52 and 53 denote controllable isolate sections associated with the horizontal registers 31, 32 and 33 to isolate the horizontal registers 31, 32 and 33 from each other in the horizontal charge transfer mode of the horizontal shift registers 31, 32 and 33. More particularly, they are constructed as shown in Fig. 9, in which numerals 51E, 52E and 53E denote control electrodes of the isolate sections 51, 52 and 53, respectively, to which the clock pulse ϕT is applied. In the present embodiment, transfer electrodes 31E', 32E' and 33E' of the horizontal shift registers 31, 32 and 33 are separated in the respective horizontal registers 31, 32 and 33 as shown although they are connected in common for each of the horizontal registers 31, 32 and 33 by well-kn wn means such as A1 substrate.

While the present embodiment shows a single-phase drive, two-phase, three-phas or even four-phase drive may be used.

The other portions are identical to the previous embodiment. A color maging system which utilizes the imaging device of the present invention may be constructed in the same manner as shown in Fig. 7.

The operation of the present embodiment is now explained. As shown in Fig. 10A, in the vertical transfer mode of the charges from the image sensing part 1 to the memory part 2, synchronous clock pulses of essentially same phase (except the clock pulse ϕS which slightly leads to the other clock pulses) which are equal in number to at least the number of vertical picture cells in the image sensing part 1 are supplied as the clock pulses ϕI, ϕS and ϕT during the time period t_1-t_2 in substantial synchronism with the vertical synchronizing signal V.SYNC so that the charges remaining in the memory part 2 are drained to the clear drain CD through the isolate sections 51–53, the horizontal registers 31–33 and the clear gate CL and the charges in the image sensing part 1 is transferred to the memory part 2 and stored therein. Then, as shown in Fig. 10B, at and after the time t_3, the clock pulse ϕT is supplied as shown to distribute the horizontal information in the last one line of the memory part 2 to the separating input section 17, the isolate sections 51–53 and the horizontal shift registers 31–33, and at and after the time t_4, the clock pulses ϕ_1, ϕ_2 and ϕ_3 are applied to the horizontal registers 31, 32 and 33 as shown to sequentially read out the information.

Regarding the information in the next and following lines of the memory part 2, the clock pulse ϕS is applied immediately before the time t_3 to shift one line of information to be read to the last line of the memory part 2 and then the above operation is repeated (Fig. 10B).

The operation during the time period t_3-t_4, that is, the operation to distribute the information in the last one line of the memory part 2 to the three horizontal shift registers 31–33 through the separating input section 17 and the isolate sections 51–53 is now explained in detail with reference to Figs. 9 and 10B. For the sake of simplification, the shift of the charge information in only three columns I, II and III of the memory part 2 shown in Fig. 9 is explained although the same operations are carried out for the columns of other three-column sets.

At time t_3, the clock pulse ϕT assumes a high level in substantial synchronism with the horizontal synchronizing signal H.SYNC and the charges stored in the portions 116, 117 and 118 in the last one line of the memory part 2 are shifted to portions 111, 114 and 115 in the separating input section 17. When the clock pulse ϕT thereafter assumes a low level, the charges in the portions 111, 114 and 115 are shifted to portions 110, 113 and 106, respectively. When the second clock

puls ϕT is applied, the charge in the portion 106 of the separating input section 17, that is, the charge initially stored in the portion 118 in the column I of the memory part 2 is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the isolate section 53, and the charges stored in the portions 111 and 114 of the separating input section 17 are shifted to the portions 108 and 106 through the portions 109 and 112, respectively. When the third clock pulse ϕT is applied, the charge in the portion 104 of the horizontal register 33 is shifted to the portion 102 of the horizontal register 32 through the portion 103 of the isolate section 52, and the charge in the portion 106 of the separating input section 17, that is, the charge initially stored in the portion 17 in the column II of the memory part 2 is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the isoate section 53. The charge in the portion 108 of the separating input section 17 is shifted to the portion 106 through the portion 107. When the fourth clock pulse ϕT is applied, the charge in the portion 102 of the horizontal register 32 is shifted to the portion 100 of the horizontal register 31 through the portion 101 of the isolate section 51 and stored therein, and the charge in the portion 104 of the horizontal register 33 is shifted to the portion 102 of the horizontal register 32 through the portion 103 of the isolate section 52 and stored therein. The charge in the portion 106 of the separating input section 17, that is, the charge initially stored in the portion 116 in the column III of the memory part 2 is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the isolate section 53 and stored therein.

In this manner, the charges stored in the last one line of the memory part 2 are distributed to the shift registers 31–33 in the groups of the columns I, II and III through the separating input part 17. Thus, if the R, G and B filter portions of a color stripe filter are arranged such that the R filter portions correspond to the column I group, the G filter portions correspond to the column II group and the B filter portions correspond to the column III group, the charges corresponding to R, G and B are stored in the horizontal registers 31, 32 and 33, respectively.

At and after the time t_4, the charges in the horizontal registers 31, 32 and 33 are read out by applying the clock pulses ϕ_1-ϕ_2. Since the clock pulse ϕT is kept at the low level at this time, the isolate sections 51–53 function as barriers so that the mixing of the charges among the horizontal registers 31, 32 and 33 in the horizontal transfer of the charg s in the horizontal registers 31, 32 and 33 is prevented.

When the charges in one horizontal line of the memory part 2 hav been read ut through the horizontal registers 31–33, the clock pulse ϕS is applied to the m mory part 2 as shown in Fig. 10B and the charges stored in the respective horizontal lines are vertically shifted by one horizontal line so that new charges are stored in the last one line, and then the operation of the time period t_3-t_4 is carried out to distribute the new one line of charges to the horizontal registers 31–33.

By repeating the above operations, the charges stored in the respective lines of the memory part 2 are separated to the respective colors and read out (OUT1-OUT 3 in Fig. 10B).

In the present embodiment, in the horizontal transfer of the input charges in the horizontal registers 31–33, the phases of the clock pulses ϕ_1, ϕ_2 and ϕ_3 to the registers 31, 32 and 33, respectively, are varied as shown in Fig. 10B so that the three color signals are produced at different phases, although the clock pulses ϕ_1-ϕ_3 may be in phase as shown by chain lines in Fig. 10B so that the three color signals are simultaneously produced. The manner of reading out the three color signals may be selected depending on the subsequent signals processing.

A further embodiment of the present invention is explained with reference to Fig. 11, which shows an improvement over the embodiment shown in Figs. 8–10. In the present embodiment, the separating input section is formed by at least using the last one line of the memory part 2 and a portion of the separating input section is provided with the function of the isolate section 53 shown in Figs. 8 and 9 so that the configuration and the manner of the control of the device are simplified and also the time period necessary for each input of one line signal to the registers 31–33 is reduced.

Referring to Fig. 11, the like numerals to those shown in Fig. 9 designate the like elements and the like numerals with primes designate the like functional means.

Numeral 17' denotes a separating input section, and numeral 17'E denotes an electrode of the separating input section 17'. The clock pulse ϕT is applied to the electrode 17'E. As shown, the separating input section 17' is formed by a region B of the last one line of the memory part 2 and a portion of the separating input section 17 has a function of the isolate section to the memory part 2, for the horizontal register 33.

The other portions are identical to Fig. 9. In the arrangement described above, when the charges have been vertically transferred from the image sensing part 1 to the memory part 2 (corresponding to the time t_2 in Fig. 10A), th charges in the last on line of the memory parts 2 are distributed in the following manner. The charge in the column I is stored in a portion 118' adjacent to the portion 105, the charge in the c lumn II is stored in a portion

117' and the charge in the column III is stored in a portion 116'. Thus, the charges in the columns I, II and III are respectively stored in the locations which respectively have different distances from the portion 105.

A readout mode starts from the above status at the time t_3 of Fig. 10B. When the clock pulse ϕT is applied, the charge of the column I of the memory part 2 stored in the portion 118' is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the separating input section 17', the charge in the portion 117' in the column II of the memory part 2 is shifted to the portion 118' of the memory part 2 through the portion 112' of the separating input section 17' and the charge in the portion 116' in the column III of the memory part 2 is shifted to the portion 108' of the separating input section 17' through the portion 109' of the separating input section 17'. When the second clock pulse ϕT is applied, the charge of the column I of the memory part 2 stored in the portion 104 of the horizontal register 33 is shifted to the portion 102 of the horizontal register 32 through the portion 103 of the isolate section 52, the charge of the column II of the memory part 2 stored in the portion 118' is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the separating input section 17', and the charge in the portion 108' of the separating input section 17' is shifted to the portion 118' of the memory part 2 through the portion 107' of the separating input section 17'. When the third clock pulse ϕT is applied, the charge of the column I of the memory part 2 stored in the portion 102 of the horizontal register 32 is shifted to the portion 100 of the horizontal register 31 through the portion 101 of the isolate section 51, the charge of the column II of the memory part 2 stored in the portion 104 of the horizontal register 33 is shifted to the portion 102 of the horizontal register 32 through the portion 103 of the isolate section 53, and the charge of the column III of the memory part 2 stored in the portion 118' of the memory part 2 is shifted to the portion 104 of the horizontal register 33 through the portion 105 of the separating input section 17'.

In this manner, the information in the last one line of the memory 2 is distributed to the horizontal registers 31–33. In the present embodiment, one line of information is distributed to the horizontal registers 31–33 with one less clock pulses than the embodiment of Fig. 9, that is, with three clock pulses ϕT. Accordingly, in the present embodiment, the number of clock puls s ϕT appli d in one less than that shown in Fig. 10B. Th waveforms of the clock pulses shown in Fig. 10A are also applicable to the present embodiment. Th operation of the horizontal charge transfer after the distribution of the charges is same as that in Fig. 9.

In the above three embodiments, the separating input sections 17 and 17' impart different amounts of delay to the respective groups of the memory part 2 such that they impart an effective delay of zero picture cell (corresponding to zero bit) to the information in the column I group of the memory part 2, an effective delay of one picture cell (corresponding to one bit) to the information in the column II group and an effective delay of two picture cells (corresponding to two bits) to the information in the column III group, in order to parallel-to-serial convert the information of the column I–III groups. The read-in of the horizontal registers 31–33 is controlled in synchronism with the serial outputs from the separating input sections 17 and 17' so that one line of information in the memory part 2 is read into the horizontal registers 31–33 by column group.

In the above embodiment, one horizontal line of information in the image sensing part 1 is divided into three parts, whch are read out by the three horizontal registers 31–33. Thus, the number of bits of each of the horizontal registers 31–33 may be approximately one third of the number of horizontal picture cells of the image sensing part 1 and hence the frequency of the clock pulses ϕ_1-ϕ_3 applied to the horizontal registers 31–33 may be reduced by a factor of approximately three. As a result, the power consumption is saved, the noise is reduced and the transfer efficiency is improved. In the embodiment of Figs. 8–11, the mixing of charges among the horizontal registers 31, 32 and 33 and the memory part 2 in the horizontal charge transfer mode is prevented by the isolate sections 51–53 or the isolate sections 51 and 52 and the separating input section 17' so that the read operation is well carried out.

While the frame transfer type two-dimensional CCD array has been specifically described, it should be understood that the present invention is equally applicable to an interline type two-dimensional CCD or CPD (charge priming device) array.

The horizontal registers serve to separately read in and read out the charges of the respective colors separated by the color separating optical member such as a color separation filter. The color separation filter may be a combination of complementary color filters. Instead of the stripe color filter, a mosaic color filter may be used.

If the number of colors separated by the color separating optical member is larger than three, the number of horizontal registers may be more than three, accordingly.

Whil the clear drain CD and the clear gate CL for clearing the unnecessary charges are provided in the present embodiment, the c lor information may be separated without them.

The separating input section 17 for the horizontal registers 31–33 may be constructed by

the gate lectrod .

In accordance with the solid state image pick-up device and the image pick-up system using the same of the present invention, the sample and hold circuit for separating the color signals is not necessary or can be extremely simplified and the mixing of the color information in reading out the color information is prevented and high quality of color information is provided. Since the readout clock frequency in the horizontal read circuit is significantly lowered, a high transfer efficiency can be maintained even if the number of horizontal picture cells of the image sensing part is increased, that is, when a horizontal resolution is increased. In addition, the noise is reduced and the power consumption is saved.

Attention is invited to copending application 8332366 (Serial No GB–A–2134347) from which this application is derived.

CLAIMS

1. A charge transfer image pick-up device for image signal processing, comprising:
an image sensing portion having a plurality of sensing cells arranged in at least one line for producing electrical information in response to incident radiation;
a storage portion having at least one row of n storage cells each for storing an electrical charge in response to a respective one of the sensing cells, said one row being classified into a plurality of storage cell groups each comprising m adjacent cells, m being no smaller than three;
one direct channel and (m-1) delay channels for each storage cell group, the (m-1) delay channels being arranged to connect (m-1) storage cells to the direct channel to which the remaining cell of the respective group is connected, each channel providing a different amount of delay, and
a read-out portion for reading out the electrical charges of one row of said storage portion and arranged to receive those electrical charges through said direct channel in each group.

2. A device as claimed in claim 1, wherein all the delay channels are controllable with a common control signal.

3. A device as claimed in claim 1 or 2, wherein the delay channels for each storage cell group have different numbers of charge transfer cells.

4. A device as claimed in claim 1, 2 or 3, wherein the read-out portion is arranged to read-out separately m groups of electrical charges of said one row.

5. A device as claimed in claim 4, wherein said m groups of electrical charges are time-sharingly supplied from said storage portion through said direct channel in each group, and each group including 1/m of the charges of said one row.

6. A device as claimed in claim 4 r 5, wherein the read-out p rtion has m read-out channels each for reading out a respective one of the groups of charges.

7. A device as claimed in claim 6, and further comprising:
m gate portions provided between the storage and read-out portions and between adjacent read-out channels.

8. A device as claimed in claim 7 when appendent to claim 4 or 5, wherein the gate portions are controllable by the same common control signal.

9. A device as claimed in claim 7 or 8, further comprising:
a clear portion for extinguishing electrical charges, the clear portion being disposd along the read-out portion at the opposite side to the said direct and delay channels; and
a further gate portion provided between said read-out portion and said clear portion, the further gate portion being controllable by the same common control signal.

10. A device as claimed in any preceding claim, wherein there is a plurality of said rows of storage cells so that the storage cells are arranged in rows and columns.

11. A device as claimed in claim 10 wherein the sensing cells are arranged in a like array of rows and columns.

12. A device as claimed in claim 11 for colour images, further comprising:
colour filter means disposed in front of the image sensing means for separating incident light into m colour components such that the columns of sensing cells having the same ordinal in n/m respective groups thereof receive the same colour light.

13. An image pick-up system, comprising:
a device as claimed in any preceding claim;
output means connected to the read-out portion for converting the electrical charges into corresponding electrical signals; and
drive means for driving the device and including means for providing said control signal.

14. A system as claimed in claim 13, wherein the output means comprises m output amplifiers.

15. A system as claimed in claim 13 or 14, further comprising:
signal processing means for processing the electrical signals provided by the output means.

16. A system as claimed in claim 14 when claim 13 is appendent to claim 12, wherein the processing means is operable to provide from the electrical signals a luminance signal and a plurality of colour signals.

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